REMARKS

Claims 68-78, 80-85 and 107-116 are presently pending in this application. Claims 79 and 117 have been cancelled without prejudice to pursuing these claims in a continuation application, and claims 68, 80, 82, 84 and 85 have been amended to clarify certain aspects of these claims. Claims 86-106 were cancelled in a previous paper.

Claims 68-85 and 107-117 were rejected in the Office Action dated 15 June 2005 as follows:

A. Claims 68-85, 107-115 and 117 were rejected under 35 U.S.C. § 103 over U.S. Patent No. 5,256,274 issued to Poris ("Poris"), Lowenheim, Frederick A., Electroplating, McGraw-Hill, pp. 416-423 ("Lowenheim"), Alkire, Richard, Transient Behavior During Electrodeposition Onto a Metal Strip of High Ohmic Resistance, Journal of Electrochemical Science, Vol. 118, No. 12, pp. 1935-1941 ("Alkire"), U.S. Patent No. 5,685,970 issued to Ameen et al. ("Ameen"), U.S. Patent No. 4,401,521 issued to Ohmura et al. ("Ohmura"), and U.S. Patent No. 5,814,557 issued to Venkatraman et al. ("Venkatraman") or U.S. Patent No. 5,863,666 issued to Merchant et al. ("Merchant").

B. Claim 116 was rejected under 35 U.S.C. § 103 over the combination of Poris, Lowenheim, Alkire, Ameen, Ohmura, Venkatraman, Merchant, and U.S. Patent No. 5,256,565 issued to Bernhardt et al. ("Bernhardt").

A. Response to Section 103 Rejection of Claims 68-85, 107-115 and 117

Independent claims 68, 80, 82, 84 and 85 were rejected over the combination of Poris, Lowenheim, Alkire, Ameen, Ohmura, and either Venkatraman or Merchant. Although these independent claims cover different subject matter, they also include several analogous elements that are relevant to this rejection. The following remarks address the patentability of claim 68 over these combinations of references with the understanding that claims 80, 82, 84 and 85 are also patentable for analogous reasons. However, the patentability of claims 80, 82, 84 and 85 is not limited to the reasons discussed below with reference to 68.

1. Claim 68 Is Directed Toward a Process For Electrochemical Deposition of Copper Onto a Semiconductor Workpiece Using a Low-Current Initiation Process Followed by an Annealing Process

Claim 68 covers processes for depositing a metal onto a semiconductor workpiece by exposing a surface of the workpiece to a plating solution including a principal metal species comprising copper. The method includes a low-current initiation procedure including applying plating power between the surface of the workpiece and an electrode in contact with the plating solution. The plating power is applied (a) at a first current density for a first period of time to deposit a first amount of metal onto the surface of the workpiece, and (b) at a second current density for a second period of time to deposit a second amount of metal onto the first amount of metal. The second current density is greater than the first current density, and a majority of the metal is deposited onto the workpiece during the second period of time. The method further includes subjecting a surface of the microelectronic workpiece to an elevated temperature annealing process at a predetermined temperature.

The method set forth in claim 68 is particularly useful for forming sub-micron copper interconnects on semiconductor workpieces. At the time of the invention, the industry sought to use copper instead of aluminum for interconnects by plating copper into trenches and/or holes in a dielectric layer. The present inventors recognized substantial improvements over previous processes by combining a plating process using a low initial current with an annealing process at an elevated temperature. The low-current initiation process electrolytically deposits copper onto the workpiece at a low initial first current density to form numerous nucleation sites for the copper deposition, and then the plating process continues at a higher second current density to deposit the majority of the copper onto the workpiece. This typically results in a copper deposit with small grain sizes that are substantially smaller than the critical dimensions of the via or trench in the dielectric layer. Excess copper may be removed from the workpiece after the plating process to electrically isolate the copper interconnect structures in the dielectric layer. The semiconductor workpiece can then be annealed to increase the grain size of the copper for improving the electrical properties of the copper deposit.

2. The Applied References Teach Annealing Procedures for Doping Non-Copper Layers or Enhancing the Ductility of Copper

Venkatraman was cited for the proposition that this reference teaches an annealing process for forming an interconnect structure formed of copper. Venkatraman, however, is actually directed to using annealing for doping an aluminum layer with copper. Referring to Figures 1 and 2 of Venkatraman, this reference discloses an interconnect structure 10 comprising a barrier layer 13, a first conductive layer 14 that fills the via portion of the interconnect, and a second conductive layer 16 that fills the line portion of the interconnect. (Column 2, lines 33-38.) The first conductive layer 14 is formed by depositing aluminum, copper, or copper alloys using a CVD process. (Column 3, lines 13-24.) The second conductive layer is then formed on the first conductive layer using a PVD process. (Column 3, lines 25-37.) Following the formation of the second conductive layer 16, "an anneal step *may be* performed *to drive some of the copper* in second conductive layer 16 into the rest of the interconnect structure 10." (Column 3, lines 38-41, emphasis added.) Venkatraman expressly states "the present invention also provides a method for doping and aluminum layer with copper to improve the reliability of the interconnect structure." (Column 4, lines 28-31.) When the teachings of Venkatraman are considered as a whole, it is clear that the annealing step is an optional step that is performed only when the second conductive layer contains copper and the first conductive layer 14 is to be doped with copper from the second conductive layer 16. As a result, Venkatraman only teaches the benefit of annealing an interconnect structure to "drive some of the copper in the second conductive layer 16 into the rest of the interconnect structure 10."

Merchant is cited for the proposition that the properties of copper deposits are improved after being annealed at 180°C. Merchant, more specifically, is directed to improving the fatigue performance characteristic of flexible laminates that have a layer of electrodeposited copper foil. Merchant teaches that conventional flexible laminates used in the electronics industry for fabricating flexible connectors, flexible circuit boards and other components are not well suited for applications that require a large number of flex cycles. To overcome this problem, Merchant teaches forming a flexible laminate having a copper foil on a flexible polymeric material by annealing the laminate at 180°C

to improve the fatigue performance. (Column 1, lines 55-65.) When the teachings of Merchant are taken as a whole, this reference teaches annealing a flexible device to enhance the ductility of the copper lines so that the device can be flexed over a large number of cycles.

3. The Rejection of Amended Claim 68 Based on Venkatraman Should Be Withdrawn Because There Is No Suggestion to Combine the Annealing Process in Venkatraman With an Electroplating Process that Deposits Copper onto Semiconductor Workpieces

In rejecting claim 68, the Examiner asserts that it would have been obvious to combine the annealing process taught by Venkatraman with a low-current initiation process taught by the combination of Poris, Lowenheim, Alkire, Ameen and Ohmura. The applicants respectfully submit that even if the combination of Poris, Lowenheim, Alkire, Ameen and Ohmura teaches a low-current initiation process, there is no suggestion to combine the annealing process in Venkatraman with any process in which copper is electrolytically deposited onto semiconductor workpieces.

Any attempt to combine the teachings of the cited references to come up with the combination of elements set forth in amended claim 68 would necessarily be based on impermissible hind-sight reasoning. As stated in C.R. Bard Inc. v. M3 systems Inc,. 48 USPQ2d, 1232 (Fed. Cir. 1998), "it is insufficient that prior art shows similar components, unless it also contains some teaching, suggestion, or incentive for arriving at the claimed structure." As stated by the Court in re Sernaker, 217 USPQ 1, 6 (Fed. Cir. 1983) in discussing an earlier case, "The lesson of this case appears to be that prior art references in combination do not make an invention obvious unless something in the prior art references would suggest the advantage to be derived from combining their teachings." The applicants submit that, as in the C.R. Bard Inc v. M3 Systems Inc. case and in the Sernaker case, the claimed invention in the present case is nonobvious over the references because there is nothing in the references to suggest that an improvement in the electrical properties of an electrolytically deposited sub-micron copper interconnect might be achieved by combining their teachings. Moreover, there is nothing in the references to suggest that the improvement defined by the combination of (a) "exposing a surface of the semiconductor workpiece to a plating solution including

a principal metal species comprising copper"; (b) "applying a plating power to electrolytically deposit metal onto the surface . . . at a first current density for a first period of time to deposit a first amount of metal onto the surface of the workpiece, and . . . a second current density for a second period of time to deposit a second amount of metal . . . wherein the second current density is greater than the first current density"; and (c) "subjecting the surface of the microelectronic workpiece to an elevated temperature annealing process at a predetermined temperature" might be achieved by combining their teachings.

To avoid an incorrect conclusion of obviousness, the Examiner must view the invention as a whole and each of the references as a whole. There are many cases that establish the requirement that the invention must be viewed as a whole and that each of the references must also be viewed as a whole when the issue of nonobviousness is confronted. In particular, the Examiner is not permitted to disregard disclosures in the references that diverge from and teach away from the invention at hand, W.L. Gore & Associates, Inc. v. Garlock, Inc., 220 USPQ 303, 311 (CAFC 1983). In the present case the problems addressed by each of the Poris, Lowenheim, Alkire, Ameen and Ohmura references are different from the problems addressed by the Venkatraman reference and also different from the problems addressed by the present invention. More specifically, none of the applied references are concerned with improving the electrical properties of copper deposits on semiconductor workpieces, and Venkatraman is limited to teaching an optional annealing step for doping an aluminum layer with copper from another layer. Because the claimed material comprises electrolytically deposited copper (e.g., highly pure copper), there is no need to drive additional copper from another layer into the electrolytically deposited copper. As a result, it follows that the annealing step taught by Venkatraman for driving copper into an underlying layer containing little or no copper would be superfluous when the underlying layer is already copper. Therefore, when taken as a whole, there is no suggestion to combine Venkatraman with the other applied references to (a) electrolytically deposit copper onto a semiconductor workpiece and then (b) anneal the copper deposit to improve the electrically properties of the copper deposit itself.

4. The Rejection of claim 68 Over the Combination of Poris, Lowenheim, Alkire, Ameen, Ohmura and Merchant Should Also Be Withdrawn Because There Is No Suggestion For Using the Annealing Process Taught in Merchant With Semiconductor Workpieces

Claim 68 is also patentable over the combination of references including Merchant. More specifically, any rejection of amended claim 68 over this combination of references would also necessarily be based on impermissible hindsight reasoning because the problems addressed by Merchant are different from the problems addressed by the other references and the present invention. The present invention is directed to improving the electrical properties of electrolytically deposited copper on a semiconductor workpiece. In contrast to this purpose, Merchant teaches annealing a flexible laminate to improve the ductility of the copper so that the copper does not fail after a large number of flex cycles. Because semiconductor workpieces are inflexible and easily broken if flexed, there is no reason to have flexible copper lines in semiconductor workpieces. As such, it follows that Merchant's annealing process for increasing the flexibility of copper lines would not be useful in semiconductor fabrication. Therefore, when the teachings of Merchant are taken as a whole, there is no suggestion for combining Merchant with the other references to anneal electrolytically deposited copper on a semiconductor workpiece.

Claim 68 is accordingly patentable over the combination of Poris, Lowenheim, Alkire, Ameen, Ohmura, and Venkatraman or Merchant. Claims 69-78 are patentable over the cited combinations of references as depending from patentable independent claim 68, and also because each of these dependent claims include additional subject matter. Therefore, the rejections of claims 68-78 should be withdrawn.

Claims 80-85 and 107-115 are also directed to methods of electrolytically depositing copper onto semiconductor workpieces or semiconductor wafers. These claims are accordingly patentable for at least the reasons explained above with reference to claim 68. The applicants further contend that several of these claims are additionally patentable over the cited references for other reasons. Therefore, the rejections of claims 80-85 and 107-115 should also be withdrawn.

B. Section 103 Rejection of Claim 116

Claim 116 was rejected under 35 U.S.C. § 103 over the combination of Poris, Lowenheim, Alkire, Ameen, Ohmura, Venkatraman or Merchant, and Bernhardt. Bernhardt does not overcome the shortcomings of the teaching of Venkatraman or Merchant explained above, and claim 116 depends from claim 85. As a result, claim 116 is patentable over the cited combination of references for the reasons explained above.

In view of the foregoing, the pending claims comply with 35 U.S.C. § 112 and are patentable over the cited art. The applicants accordingly request reconsideration of the application and a Notice of Allowance. If the Examiner has any questions or believes a telephone conference would expedite prosecution of this application, the Examiner is encouraged to call Paul T. Parker at (206) 359-3258.

Respectfully submitted,
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